REMARKS

This paper is presented in response to the Office Action. Claims 1, 20, and 28 are presented in this paper. Claims 1-42 remain pending in the application.

Reconsideration of the application is respectfully requested in view of the aforementioned amendments to the claims and the following remarks. For the convenience and reference of the Examiner, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. General Considerations

Applicants note that the remarks and amendments presented herein have been made merely to clarify the claimed embodiments from elements purported by the Examiner to be taught by the cited references. Such remarks, or a lack of remarks, and amendments are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicants reserve the right to challenge the purported teaching and prior art status of the cited references at any appropriate time.

In addition, the remarks herein do not constitute, nor are they intended to be, an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed herein are presented solely by way of example. Consistent with the foregoing, the discussion herein is not intended, and should not be construed, to prejudice or foreclose contemporaneous or future consideration, by the Applicants, of additional or alternative distinctions between the claims of the present application and any references cited by the Examiner, and/or the merits of additional or alternative arguments.

II. Claim Objections

The Examiner has objected to claims 1 and 28 for various informalities. In particular, the Examiner has stated, "As per claims 1 and 28, it is believed the phrase 'memory, and a plurality of processor[s] and one or more' should read –memory, a plurality of processors and one or more- and has been treated as such for the rest of this office action." *Office Action, page 3.* Notwithstanding these allegations, Applicants believe that no amendment to claims 1 and 28 is required. Moreover, the Examiner has failed to provide any evidence in support of the objection. Accordingly, Applicant

respectfully declines to amend claims 1 and 28, and submits that the objection to the specification should be withdrawn.

III. Claim Rejections under 35 U.S.C. § 103

Applicants respectfully note at the outset that in order to establish a *prima facie* case of obviousness, it is the burden of the Examiner to demonstrate that three criteria are met: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Manual of Patent Examining Procedure ("MPEP") § 2143.*

a. claims 1-6 and 9-33

The Examiner has rejected claims 1-6 and 9-33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,401,176 to Fadavi-Ardekani et al. (*"Fadavi-Ardekani"*) in view of U.S. Patent No. 5,893,153 to Tzeng et al. (*"Tzeng"*). Applicants respectfully disagree.

Each of the rejected independent claims 1, 20, and 28 recites a "memory controller" that is configured to perform an act of "allotting a first division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a first processor such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles."

In connection with the rejection of independent claims 1, 20, and 28, Applicants understand that the Examiner has characterized an "arbiter 102" of *Fadavi-Ardekani* as corresponding to the "memory controller," a "super agent A" of *Fadavi-Ardekani* as corresponding to the "first processor," and a "shared synchronous memory 200" of *Fadavi-Ardekani* as corresponding to the "system memory." *See Office Action, page 4.* In asserting that the "super agent A" of *Fadavi-Ardekani* satisfies the "memory access is guaranteed" limitation of the "first processor," the Examiner has stated that "the 'super agent' is not required to arbitrate for access to memory with the other agents (Column 5, lines 13-16); therefore, the "super agent" is guaranteed access to memory." *Office Action, page 4.*

In light of the foregoing, it thus appears to be the position of the Examiner that *Fadavi-Ardekani* discloses that the arbiter 102/202 performs or is configured to perform an act of "allotting a first division of each of a plurality of memory access cycles" for the "super agent A." If, however, Applicants' understanding on this point is incorrect, Applicant respectfully requests that the Examiner provide suitable clarification.

Despite the assertions of the Examiner, however, it appears from Figure 3 of *Fadavi-Ardekani* that any division of "memory access cycles" allotted and guaranteed to the super agent A are not allotted and guaranteed by the arbiter 202. *Fadavi-Ardekani* confirms this understanding, stating:

> [I]t is within the principles of the present invention as will be discussed in more detail herein below to designate one of the plurality of agents as a super agent and allow that super agent to communicate with the shared synchronous memory 200 without requiring that super agent to arbitrate for ownership of the shared synchronous memory 200. In this case, all other agents would monitor the super agent's communications with the shared synchronous memory 200.
>
> For instance, FIG. 3 shows a plurality of agents including a super agent A and a non-super agent B wherein the super agent A is allowed to communicate with the shared synchronous memory 200 *without* arbitration.
>
> In particular, FIG. 3 shows a shared synchronous memory 200 which is accessible by both a super agent A and a non-super agent B. The super agent A has direct access to the shared synchronous memory 200, while the non-super agent B accesses the shared synchronous memory 200 under the control of an arbiter and switch [202]. Thus, the super agent A obtains access to the shared synchronous memory 200 directly via a communication path 220, while the non-super agent B requests access to the shared synchronous memory 200 via the arbiter and switch 202 using communication paths 222a, 222b and 222c.

Column 5, lines 26-49 (emphasis added).

In light of the disclosure of *Fadavi-Ardekani* that "The super agent A has direct access to the shared synchronous memory 200, while the non-super agent B accesses the shared synchronous memory 200 under the control of an arbiter and switch [202]," that reference appears to contradict the assertion of the Examiner that the arbiter 202 can be characterized as allotting "memory access cycles" to the super agent A, since it is clear that the super agent A is not "under the control of an arbiter and switch [202]" as the Examiner appears to allege. See, *column 5, lines 41-44 (emphasis added).*

The rejection of independent claims 1, 20, and 28 is problematic for other reasons as well. For example, the Examiner has alleged that "Fadavi-Ardekani discloses…a system memory…a plurality of processors… that each access the system memory through a memory controller." *Office Action, pages 3-4 (emphasis added).* Despite the assertions of the Examiner that the "super agent A" accesses the memory 200 "through" the arbiter 202, Applicants respectfully note that Figure 3 and the portions of *Fadavi-Ardekani* cited above clearly disclose that "the super agent A obtains access to the shared synchronous memory 200 directly via a communication path 220," and not through the arbiter 202. *Column 5, lines 44-46 (emphasis added).*

In light of the disclosure of *Fadavi-Ardekani*, contradicting the assertion of the Examiner that the super agent A accesses the memory 200 through the arbiter 202, it is not at all clear to Applicants how

Fadavi-Ardekani can properly be characterized as disclosing "a plurality of processors [including the first processor] ... that each accesses the system memory through a memory controller" as required by claims 1 and 28 or "a plurality of processors [including the first processor] that each accesses the system memory through the memory controller" as required by claim 20.

As the foregoing makes clear, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1, 20, and 28, at least because the Examiner has failed to establish that *Fadavi-Ardekani* and *Tzeng*, either alone or in combination, teach or suggest all the claim limitations of claims 1, 20, and 28. Applicants thus respectfully submit that the rejection of claims 1, 20, and 28, as well as the rejection of corresponding dependent claims 2-6, 9-19, 21-17 and 29-33, should be withdrawn.

b. claims 7-8 and 34-42

The Examiner has rejected claims 7-8 under 35 U.S.C. § 103(a) as being unpatentable over *Fadavi-Ardekani* and *Tzeng* and further in view of U.S. Patent No. 6,275,885 to Chin et al. ("*Chin*"). The Examiner has also rejected claims 34 and 40-42 under 35 U.S.C. § 103(a) as being unpatentable over *Fadavi-Ardekani* and *Tzeng* and further in view of an assertion by the Examiner that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the controller as being claimed in claim 30 in a laser transmitter/receiver..." Finally, the Examiner has rejected claims 35-39 under 35 U.S.C. § 103(a) as being unpatentable over *Fadavi-Ardekani* and *Tzeng* and further in view of an assertion by the Examiner that "it would have been obvious to a person of ordinary skill in the art to apply the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G..."

Applicants respectfully submit that insofar as the rejection of claims 7-8 and 34-42 relies on the characterization of *Fadavi-Ardekani* advanced by the Examiner in connection with the rejection of claims 1-6 and 9-33, such rejection lacks an adequate foundation, for at least the reasons outlined at **III.a** above, and should accordingly be withdrawn.

IV. Request for Examiner Affidavit

In connection with the foregoing, Applicants note that it appears that the Examiner is relying on personal knowledge as a basis for rejecting claims 34-42. Particularly, the Examiner has stated, "However, the examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the controller as being claimed in claim 30 in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver." The Examiner has also stated, "At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to apply the controller of claim

30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G…One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any memory size because the combination Fadavi-Ardekani and Tzeng provides a method/system/controller to control accesses to memory by a plurality of processors and other peripheral or I/O devices, regardless of the size of the memory."

However, the Examiner has not identified any references or other materials as being obvious to combine with the purported teachings of the other cited references. In view of the foregoing, and pursuant to 37 C.F.R. 1.104(d)(2), Applicants hereby respectfully request an Examiner affidavit that: (i) specifically identifies any and all reference(s), other than those that have been specifically cited by the Examiner, upon which the obviousness rejection of claims 34-42 is based; and (ii) provides complete details concerning the reasoning and analysis of the Examiner concerning those references as those references are purported to apply to the rejection of claims 34-42.

V. Amendments to Claims 1, 20 and 28

Applicants note that the amendment herein to claims 1, 20, and 28 have not been made in response to any rejection or objection posed by the Examiner, but rather simply to refine the language of those claims. In this regard, it should be noted that Applicants have broad discretion to choose and modify the language of a claim and, moreover, various patentable expressions of comparable claim scope lie within the bounds of such discretion. Because the amendments to claim 1, 20 and 28 fall within the bounds of that discretion, such amendments are not related to patentability of those claims.

CONCLUSION

In view of the remarks submitted herein, Applicants respectfully submits that each of the pending claims 1-42 in this application is in condition for allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that could be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 30th day of October, 2006.

Respectfully submitted,

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